Electronic Version
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Claims

[c1] A semiconductor structure formed on a substrate, comprising a shallow trench isolation having at least one overhang selectively configured to prevent oxidation induced stress in a determined portion of the substrate.

[c2] The semiconductor structure of claim 1, further comprising:
a device having a source and a drain with a direction of current flow;
wherein one of the at least one overhang is selectively configured to prevent oxidation induced stress in a direction parallel to the direction of current flow.

[c3] The semiconductor structure of claim 1, further comprising:
a device having a source and a drain with a direction of current flow;
wherein one of the at least one overhang is selectively configured to prevent oxidation induced stress in a direction transverse to the direction of current flow.

[c4] The semiconductor structure of claim 1, wherein:
the determined portion of the substrate is an Si-SiO_2 in-

terface adjacent to the shallow trench isolation; and
the at least one overhang extends beyond the Si-SiO_2 interface, preventing oxidation at or near the Si-SO_2 interface.

[c5] The semiconductor structure of claim 1, further comprising:
a first device having a source and a drain with a direction of current flow for the first device; and
a second device having a source and a drain with a direction of current flow for the second device;
wherein the shallow trench isolation includes
a first shallow trench isolation side for the first device having at least one overhang configured to prevent oxidation induced stress in a direction parallel to the direction of current flow for the first device; and
a second shallow trench isolation side for the first device having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the first device; and
a third shallow trench isolation side for the second device having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the first device.

[c6] The semiconductor structure of claim 5, wherein the shallow trench isolation further includes a fourth shallow

trench isolation side for the second device, the fourth shallow trench isolation being devoid of an overhang.

[c7] A semiconductor structure formed on a substrate, comprising:
an n-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain; and
a first shallow trench isolation for the n-channel field effect transistor, the first shallow trench isolation having a first shallow trench isolation side, the first shallow trench isolation side having at least one overhang configured to prevent oxidation induced stress in a direction parallel to the direction of current flow for the n-channel field effect transistor.

[c8] The semiconductor structure of claim 7, wherein the first shallow trench isolation for the n-channel field effect transistor further comprises:
a second shallow trench isolation side being transverse to the first shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the n-channel field effect transistor.

[c9] The semiconductor structure of claim 8, further comprising:

a p-channel field effect transistor, the p-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain;
a second shallow trench isolation for the p-channel field effect transistor having a third shallow trench isolation side, the third shallow trench isolation side being devoid of an overhang; and
the second shallow trench isolation for the p-channel field effect transistor further having a fourth shallow trench isolation side, the fourth shallow trench isolation side being transverse to the third shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the p-channel field effect transistor.

[c10] The semiconductor structure of claim 9, wherein the overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow prevents a degradation of hole mobility.

[c11] The semiconductor structure of claim 9, wherein:
the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side of the first shallow trench isolation for the n-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the first shal-

low trench isolation would affect performance of the n-channel field effect transistor, and
the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side of the first shallow trench isolation for the n-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the second shallow trench isolation would affect performance of the n-channel field effect transistor.

[c12] The semiconductor structure of claim 1, wherein the overhang includes a T-shaped structure.

[c13] The semiconductor of claim 12, wherein the determined portion of the substrate is an Si-SO_2 interface adjacent to the shallow trench isolation.

[c14] The semiconductor of claim 13, wherein the overhang includes a horizontal portion that extends beyond the Si-SiO_2 interface by about 0.01 microns to 0.5 microns.

[c15] The semiconductor structure of claim 9, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side for the second shallow trench isolation for the p-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the fourth

shallow trench isolation side would affect performance of the p-channel field effect transistor.

[c16] The semiconductor structure of claim 15, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side is less than or equal to about 5.0 microns.

[c17] The semiconductor structure of claim 11, wherein the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side is less than or equal to about 5.0 microns.

[c18] The semiconductor structure of claim 12, wherein the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side is less than or equal to about 5.0 microns.

[c19] A process of forming a semiconductor structure, comprising:
forming a structure comprised of a silicon layer, a silicon dioxide layer on the silicon layer, and a silicon nitride layer on the silicon dioxide layer;
forming a shallow trench isolation on the structure having a first shallow trench isolation side having at least one overhang configured to prevent oxidation induced stress in a first determined direction, and a second shal-

low trench isolation side being transverse to the first shallow trench side and being devoid of an overhang.

[c20] The process of claim 19, wherein the step of forming the shallow trench isolation includes:
etching a portion of the silicon nitride layer, the silicon dioxide layer and the silicon layer to form a trench;
etching sidewall portions of the silicon nitride layer in the trench creating a recession of the silicon nitride layer relative to the trench for the first shallow trench isolation side; and
depositing silicon dioxide into the trench and recession to form the shallow trench isolation with a first shallow trench isolation side having an overhang.

[c21] The process of claim 20, further comprising a step of forming a field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain.

[c22] The process of claim 21, wherein the distance from the gate of the field effect transistor to the first shallow trench isolation side is less than or equal to a distance within which oxidation induced stress adjacent to the first shallow trench isolation side would affect performance of the field effect transistor.